ABSTRACT OF THE DISCLOSURE

An area for layout of a plurality of I/O cells (called an "I/O area") is provided in the peripheral portion of a chip and signal wirings for ~~transfer a test signal~~ transferring test signals to the I/O cells are provided in the layout direction of the I/O cells. At least one [[of]] empty ~~cells~~ cell provided in the I/O area at ~~positions~~ a position where [[the]] I/O cells are not provided has a repeater circuit which constitutes a transfer path for the test signal. The repeater circuit receives the test signal and outputs the test signal. This structure provides a suitable semiconductor integrated circuit device adaptable for an ASIC or ~~so~~ the like, which can adjust the delay of a test signal to be transferred along the chip's peripheral portion by suppressing an increase in the delay and degradation in waveform depression.